	Application No.	Applicant(s)	
Notice of Allowability	09/685,272	DOWLING, ERIC M.	
	Examiner	Art Unit	
	Tuan A Vu	2124	
The MAILING DATE of this communication apperall claims being allowable, PROSECUTION ON THE MERITS IS herewith (or previously mailed), a Notice of Allowance (PTOL-85) NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT R of the Office or upon petition by the applicant. See 37 CFR 1.313. 1. This communication is responsive to 4/22/2004. 2. The allowed claim(s) is/are 24-29,42-74 and 77-79. 3. The drawings filed on 10/09/2000 are accepted by the Examulation of the accepted by the Examulation of the communication of the communication of the priority documents have	ears on the cover sheet w (OR REMAINS) CLOSED i) or other appropriate comm IGHTS. This application is 3 and MPEP 1308. miner. miner. the been received.	ith the correspondence address in this application. If not included unication will be mailed in due course subject to withdrawal from issue at the	: THIS e initiative
2. Certified copies of the priority documents have			
 3. Copies of the certified copies of the priority do International Bureau (PCT Rule 17.2(a)). * Certified copies not received: 		·	
Applicant has THREE MONTHS FROM THE "MAILING DATE" noted below. Failure to timely comply will result in ABANDONN THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.	of this communication to file I/ENT of this application.	e a reply complying with the requireme	ents
5. A SUBSTITUTE OATH OR DECLARATION must be subm INFORMAL PATENT APPLICATION (PTO-152) which giv			OF
 CORRECTED DRAWINGS (as "replacement sheets") must (a) including changes required by the Notice of Draftspers 1) hereto or 2) to Paper No./Mail Date (b) including changes required by the attached Examiner' Paper No./Mail Date Identifying indicia such as the application number (see 37 CFR 1 each sheet. Replacement sheet(s) should be labeled as such in 67. DEPOSIT OF and/or INFORMATION about the deposition of the control of the contro	son's Patent Drawing Revie . s Amendment / Comment o .84(c)) should be written on the header according to 37 C	r in the Office action of he drawings in the front (not the back) R 1.121(d).	
attached Examiner's comment regarding REQUIREMENT			
Attachment(s) 1. ☐ Notice of References Cited (PTO-892)	5 ☐ Notice of It	formal Patent Application (PTO-152)	
Notice of Neterences Cred (1 10-032) Notice of Draftperson's Patent Drawing Review (PTO-948)		ummary (PTO-413),	
3. Information Disclosure Statements (PTO-1449 or PTO/SB/0	Paper No.	/Mail Date Amendment/Comment	
Paper No./Mail Date 4.	8. 🛭 Examiner's	Statement of Reasons for Allowance	;
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U.S. Patent and Trademark Office PTOL-37 (Rev. 1-04) Art Unit: 2124

DETAILED ACTION

1. This action is responsive to the Applicant's response filed 4/22/2004.

As indicated in Applicant's response, claims 34-41 have been canceled and no new claim added. Claims 24-29, 42-74, and 77-79 are pending in the office action.

Double Patenting

2. In view of the submitted Terminal Disclaimer filed as per 4/22/2004, the Double Patenting rejection is herein withdrawn. The disclaimer has been noted as having entered and accepted as per July 2, 2004.

EXAMINER'S STATEMENT OF REASONS FOR ALLOWANCE

3. Claims 24-29, 42-74, and 77-79 are allowed.

The following is an examiner's statement of reasons for allowance.

The prior art of record, taken alone or in combination fails to teach or suggest the following claimed features:

A method for processor comprising (i) a programmable address arithmetic unit (PAAU); (ii) a first software instructions comprising a fixed set of instructions to implement an algorithm and at least one user-defined addressing mode in the PAAU; and (iii) a configuration data or program code adapted to configure operation of at least one user-defined addressing mode in the PAAU, wherein instructions executed in the fixed set operate with instruction data from the configuration of said user-defined addressing mode, as recited in claim 24, 42, 51, 60, 69, 74, and 77.

(iv) A computerized system with a processor comprising a programmable address arithmetic unit and a first software instructions comprising a fixed set of instructions to implement an algorithm and at least one user-defined auto-update addressing mode; a

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configuration data adapted to configure operation of at least one user-defined auto-update addressing mode in the PAAU, wherein op-code execution makes reference to an operand using the user-defined auto-update addressing mode instruction, by way of whose successive execution results in an addressing pattern, wherein the addressing pattern is non-linear and dependent on the application algorithm, and is using less cycles than would be possible by using a combination of instructions involving the fixed set of addressing modes as recited in claim 79.

Holiday (USPN: 6,421,739) discloses implementing user-defined address mapping function in a Programmable Logic Array (PLA) interconnect unit and a high-level definition language to implement the algorithm for operation of a target circuitry in a simulation system but fails to disclose a PAAU as in (i), a fixed instructions set to implement user-defined addressing mode in that PAAU as in (ii) and a configuration code to configure operation of said user-defined addressing mode in said PAAU as in (iii) and (iv).

Baxter, (USPN: 6,182,206) discloses in a emulation system dynamic reconfiguring of memory organization in a PLA and re-programmable address operate unit to perform address-related operations coupled with the instructions fetched by the emulated processor, but does not disclose a fixed instructions set to implement user-defined addressing mode in a PAAU and a configuration code to configure operation of said user-defined addressing mode in said PAAU, wherein instructions executed in the fixed set operate with instruction data from the configuration of said user-defined addressing mode as recited in (iii) and in (iv).

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Liao, "Storage Assignment to Decrease Code Size", discloses reducing of generated code for DSP environment by subsuming the address arithmetic into auto-increment and auto-decrement modes with register use and optimizing heuristic algorithm; but fails to disclose a PAAU as in (i), a fixed set of instructions as in (ii) and a configuration code as in (iii) and (iv).

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tuan A Vu whose telephone number is (703)305-7207. The examiner can normally be reached on 8AM-4:30PM/Mon-Fri.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kakali Chaki can be reached on (703)305-9662.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

or faxed to:

(703) 872-9306 (for formal communications intended for entry)

or: (703) 746-8734 (for informal or draft communications, please consult Examiner before using this number)

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Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington. VA., 22202. 4th Floor(Receptionist).

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

VAT July 7, 2004

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KAKALI CHAXI SUPERVISORY PATENT EXAMINER TECHNOLOGY CENTER 2100